UNIVERSITY OF MUMBAI

OFFICE REGISTER FOR THE B.E. (ELECTRONICS ENGINEERING)(SEM VII)(REVISED TO CBGS COURSE) EXAMINATION HELD IN NOVEMBER 2018

COLLEGE/CENTRE : 561 PIITE MARCH 18, 2019

SEAT NO.	NAME OF CANDIDATE / CENTRE	PP1 WR	PP1 TW	PP1 O/P	PP2 WR	PP2 TW	PP2 O/P	PP3 WR	PP3 TW	PP3 O/P	PP4 WR	PP4 TW	PP4 O/P	PP5 WR	PP5 TW	PP5 O/P	PP6 TW	PP6 O/P	TOTAL	RESULT
		100	25	25	100	25	25	100	25	25	100	25	25	100	25	25	25	25	800	
		40	10	10	40	10	10	40	10	10	40	10	10	40	10	10	10	10		
11177016	KAUL MOHIT MOHANLAL MOHAN A	AA	20+	22+	53+	17+	20+	04F	17+	20+	35F	15+	24+	00Z	14+	20+	24+	23+	328	F
11177017	MAHAMUNI PUSHKAR VASUDEO KIRTIMANGAL	40+	19+	16+	50+	20+	20+	40+	18+	17+	59	20+	20+	47+	19+	20+	21+	19+	465	P RLE

01. BASIC VLSI DESIGN (SEM-6)
02. FILTER DESIGN
03. POWER ELECTRONICS - II
04. COMPUTER COMMUNICATION NETWORKS
05. ELECTIVE-I : 5:DIGITAL IMAGE PROCESSING
06. PROJECT-A

05. ELECTIVE-I : 38:DIGITAL IMAGE PROCESSING DESIGN

#:O.229; @:O.5042; *:O.5045;RCC:O.5050; +:MARKS CARRIED; /:FEMALE;NULL:NULL & VOID AS NO MARKS IN T.W.;P:PASSES;F:FAILS;A:ABSENT;
--:NOT APPLICABLE;E:EXEMPTION CAN BE CLAIMED; RR:RESERVED; ADC:ADMN. CANCELLED; PPR: PASSED PREVIOUSLY; RLE- LOWER EXAM NOT CLEAR;
~ : DYSLEXIA BENEFIT